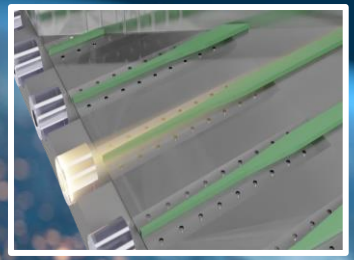
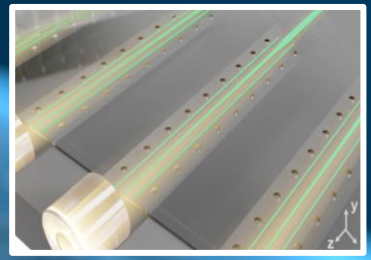
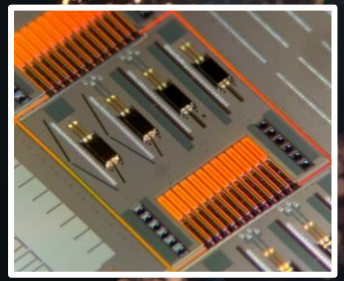
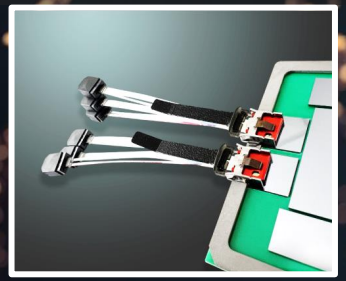
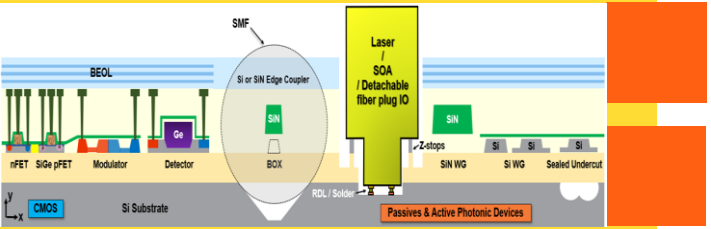




High-performance and diverse optical I/O solutions on a 300-mm monolithic CMOS-SiPh platform


Yusheng Bian*, PhD
*Director/Distinguished Engineer & Master Inventor
GlobalFoundries
*yusheng.bian@gf.com
2025



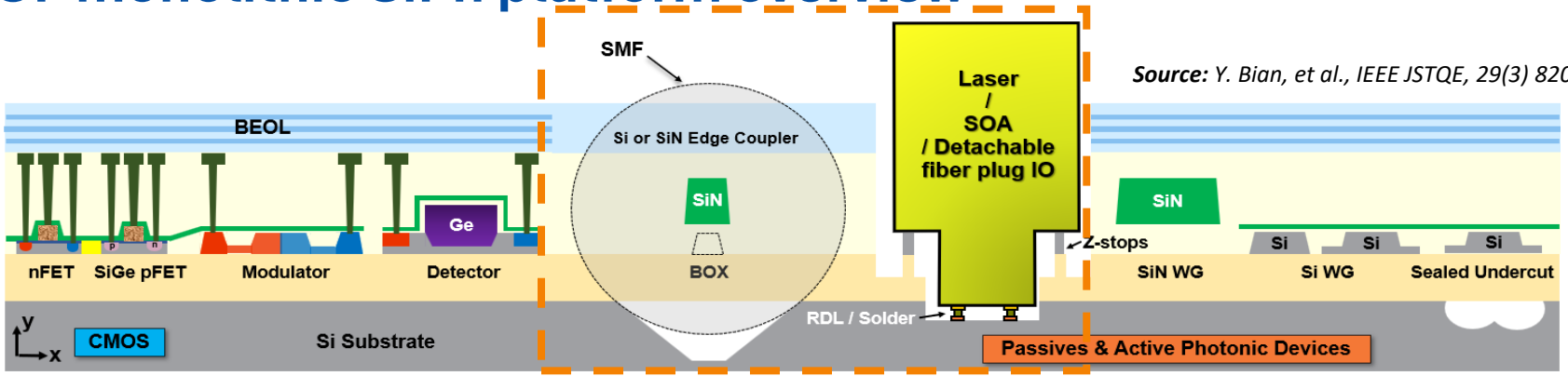
GF Fotonix™: Trusted Production Solution

GlobalFoundries (GF) is the world's third-largest semiconductor foundry by revenue

Market Segments	Computing, mobile, wired and wireless infrastructure. **Trusted Foundry**
Employees	~3,000
Differentiated Technologies	14/12LP, 12LP+, 12RF, 45RF **Silicon Photonics**
Operating since	2011
Manufacturing capacity	500k (300mm wafers/year)

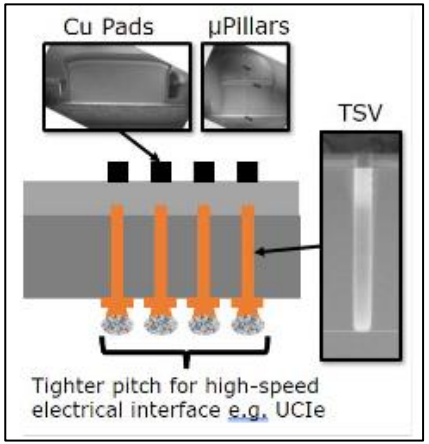
Fab8 Malta, NY

GF monolithic SiPh platform overview



Source: *Y. Bian, et al., IEEE JSTQE, 29(3) 8200519 (2023)*

- **Monolithic integration of 45nm class RFCMOS & std cell digital logic**
- **Fiber Attach:** **250/127um** pitch passive V-groove, 32+ array size
- **Photonic Device Highlights**
  - Comprehensive O-band photonic library
  - 56Gbaud PD and modulators. 112Gbaud in development (***120 Gbaud PD – CLEO 2025 PDP****)
  - 300GHz class analog mixed signal CMOS with standard cell digital library
  - Enhanced high power SiN device suite, including athermal cWDM
  - Micro-ring dWDM ring filters with high efficiency sealed undercut (airgap) heaters
  - Polarization management, PSRs, low PDL
- **Cu Pillar & TSV** (<55um pitch) supports 2.5D & 3D form-factors
- **Flows support hybrid EIC** only or as combination of hybrid EIC + monolithic EPIC
- **State-of-art Co-design PDK:** Hardware-based models, 105C, self-heating, optical power
- **Custom design support:** freeform / curve-linear GDS accepted, stack-up guide
- **300mm patterning:** immersion lithography Si WG, Optimized OPC for photonic layouts



** Y. Bian, et al., CLEO, Postdeadline 104_7 (2025)*

GF Fotonix™: Technology Solution

Legend:
CMOS
Optical
Bold = New features

MZI modulators

Micro-ring modulators

dWDM Ring filters

High BW Ge EPI PD

*Passive library: SOI & **SiN Ridge**, rib WGs, bends, tapers, directional couplers, **MMIs**, cross, absorbers, …*

BEOL passives, inductors, VNcap

RF CMOS, standard cell, GPIO, ESD, eFuse, TIA, driver, precision resistor

300mm CMOS-SiPh Monolithic platform

Thermal phase shifters w/ **sealed airgap undercut**

4x MUX/DEMUX Mzi filters

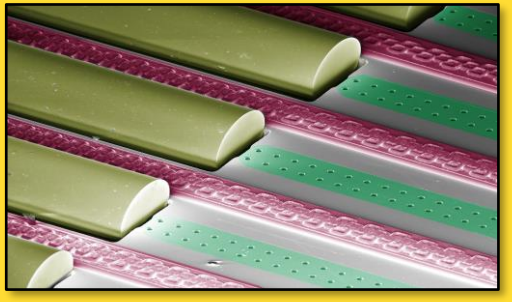
2.5D & 3D integration solutions (Cu Pillar & Cu Rx Pads &TSV)

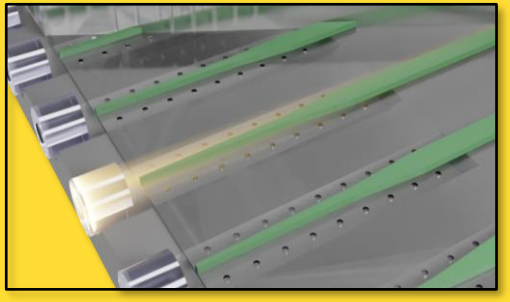
Top grating couplers

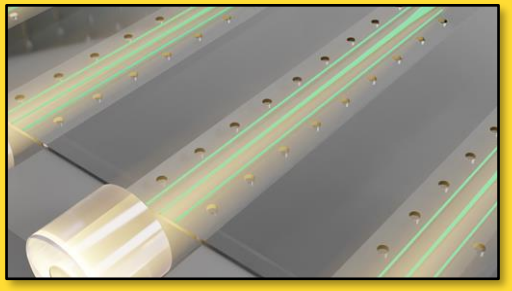
Passive & active fiber attach with Si or **SiN SSC**

Direct laser attach

Polarization splitter & polarization rotator

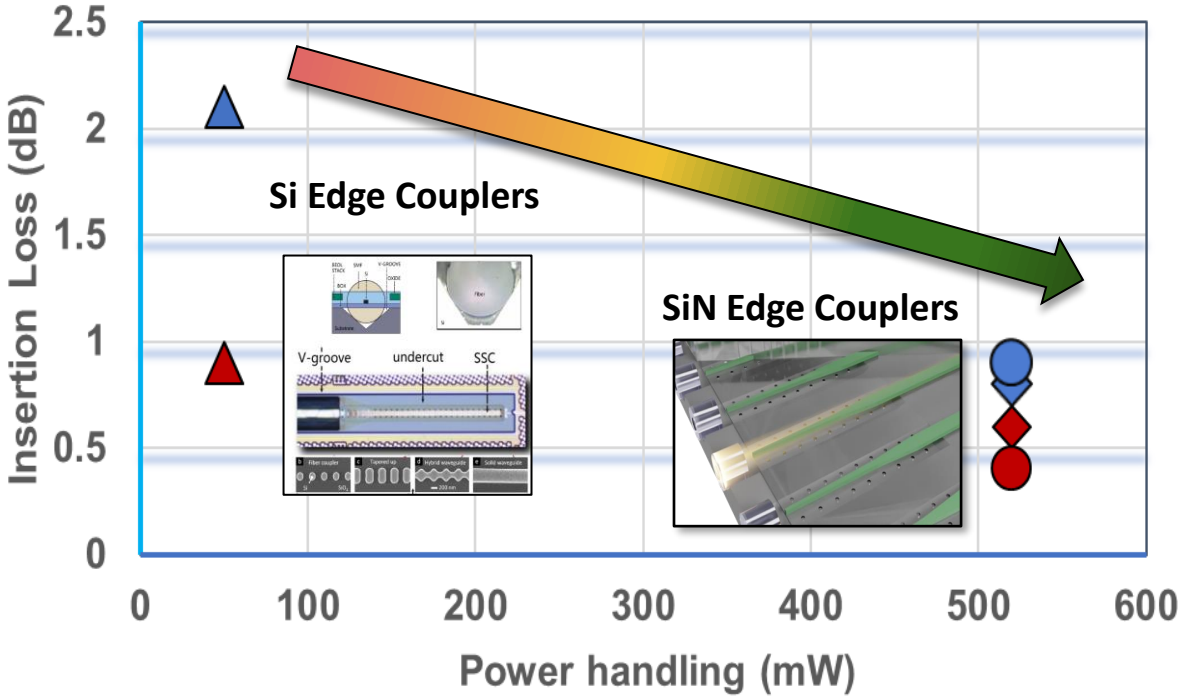






1	GF monolithic SiPh platform
2	V-groove-based fiber attach
3	Detachable I/O coupler
4	Summary and outlook

Towards low-loss, high power, self-aligned fiber attach solution

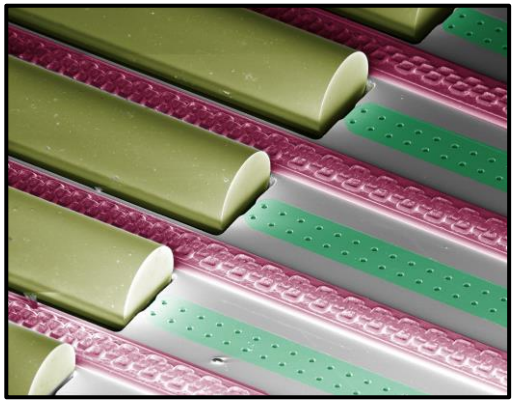


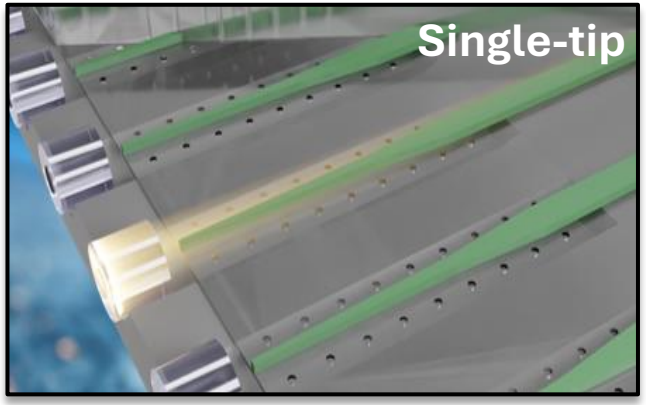
- **Need for high-performance fiber attach**:
  - High transmission efficiency (**< 1 dB**)
  - Low polarization dependent loss (TE vs TM) **< 0.5 dB**
  - Low back reflection (IEEE 802.3cu-2021: **ORL < -26 dB** for overall **TX** or **RX**)
  - Broadband operation (e.g. O-band, C-band)
  - **High power handling (e.g. > 100 mW)**
  - Self alignment (e.g. V-groove)

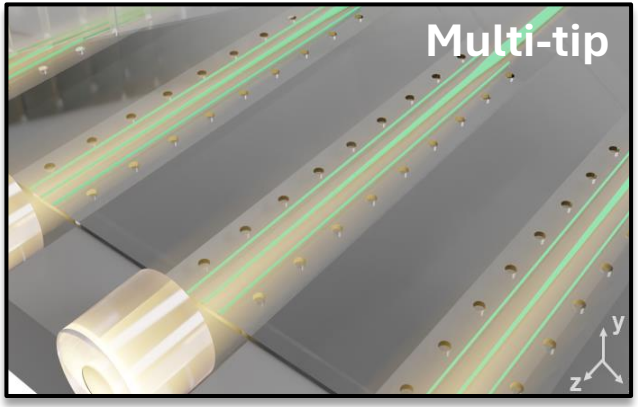
- **Solution**: switching from **Si edge coupler to SiN edge coupler**

Source: *Y. Bian, et al., OFC M3C.3 (2023); Y. Bian, et al., CLEO AA129.1 (2025)*

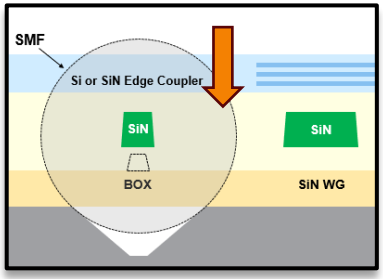
Monolithically integrated SiN edge couplers (single/multi-tip)







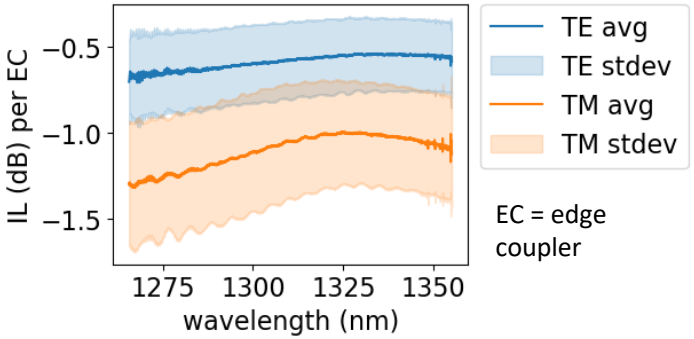
- **Integration of high-performance SiN edge coupler on the monolithic SiPh platform**
  - Leveraging existing MOL SiN waveguide layer which has good high power handling capability
  - **193-nm DUV litho** and **advanced free-form OPC** ensuring high pattern fidelity and minimized loss
  - Advanced **TMAH module** forming **V-groove** with **precisely controlled shape** and **dimensions**
  - **Undercut below the spot size converter** (SSC) preventing optical leakage into the substrate
  - BEOL replaced with **thick TEOS cladding** for improved mode matching with SMF
  - Additional process optimizations **preventing SiN SSC from being damaged** during BEOL removal
  - **Simultaneous integration of Si and SiN edge couplers** on the same monolithic PIC now becoming possible
  - SSC geometry and shape optimization enabling **improved mode matching** and **reduced conversion loss**



Source: *Y. Bian, et al., OFC M3C.3 (2023)*

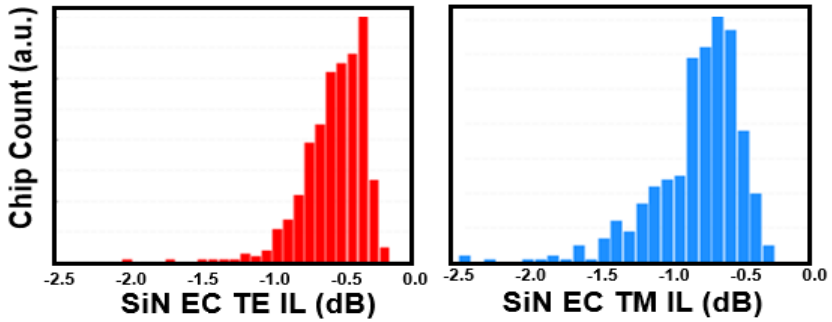
16-channel 250µm-pitch SiN EC with low IL and flat through-band loss

Flat wavelength response across large sample size

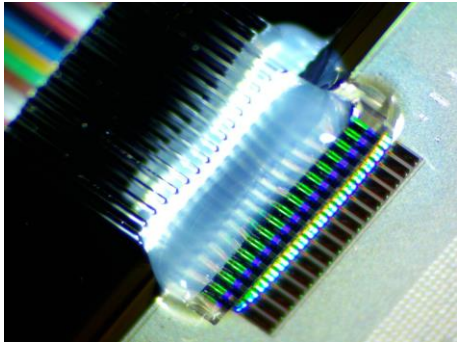


EC = edge coupler

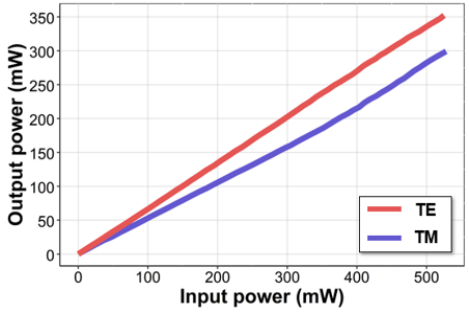
Large sample size of passive fiber attach shows low average IL

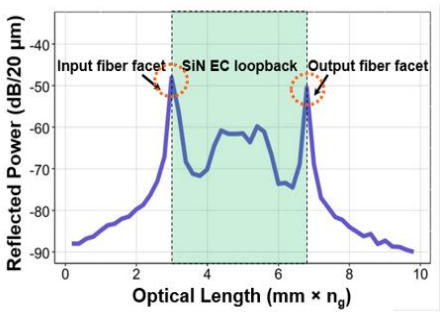


16-channel 250µm pitch passive fiber attached to 16-channel V-groove array

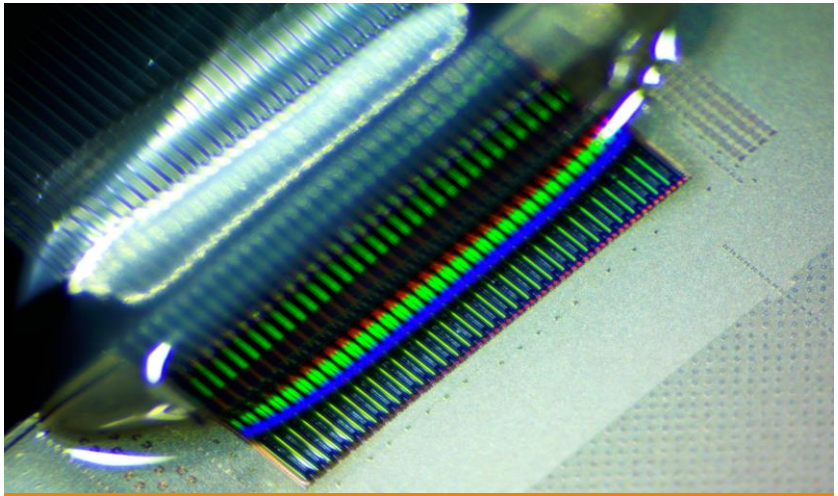


HP ramps show no roll-off in insertion loss up to 520 mW

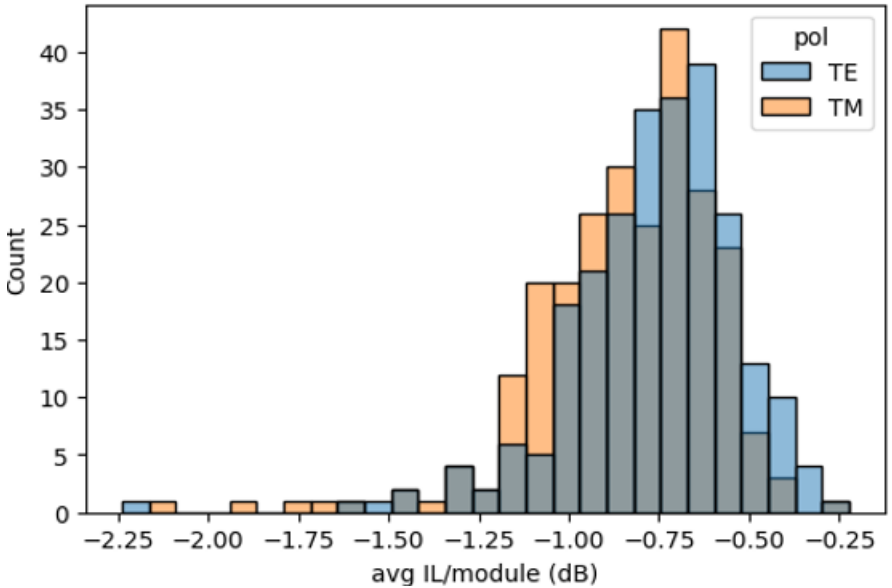




32-channel 127µm-pitch SiN EC with low IL/PDL/though-band performance

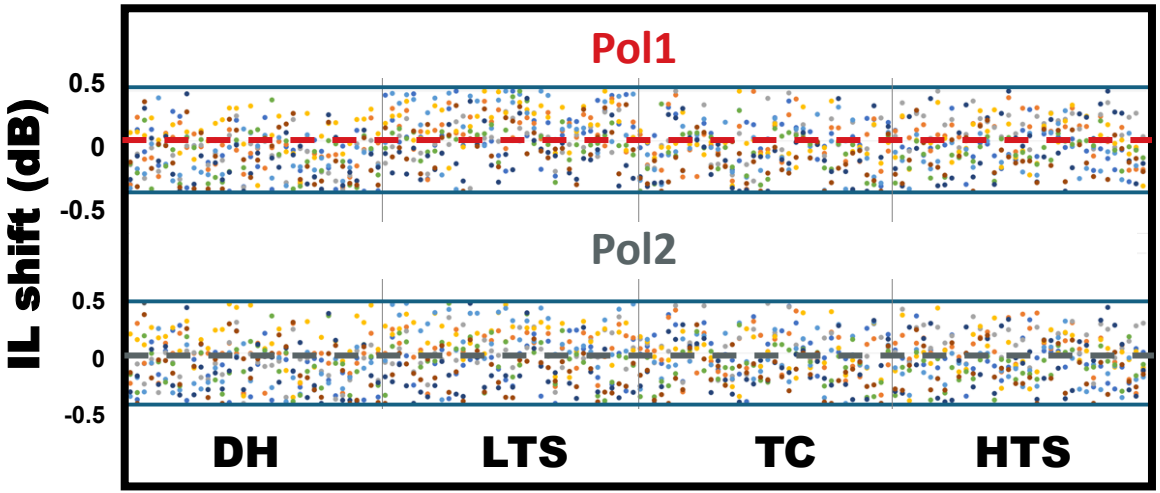


Module with 32-channel fiber ribbon attached



- Sub-1 dB TE and TM IL and < 0.1 dB PDL demonstrated on 32-channel 127µm-pitch Vgroove array, occupying the same footprint as a 16-channel 250µm-pitch array
- 2X Edge bandwidth/beachfront density by doubling the physical port count

127-um pitch SiN edge coupler full reliability assessment

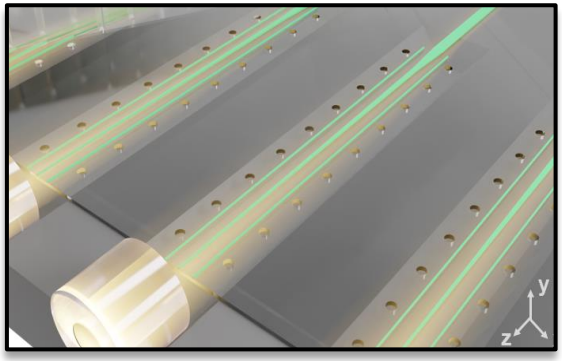


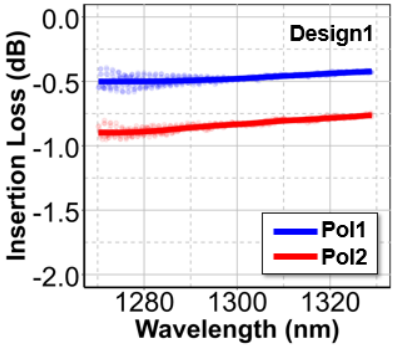
Test item (36 modules)	Result
LTS (-40°C, 72hrs)	Pass
HTS (105°C, 2000 hrs)	Pass
TC (-40°C to 105°C, 500 cycles)	Pass
DH (85°C/85% RH, 500 hrs)	Pass

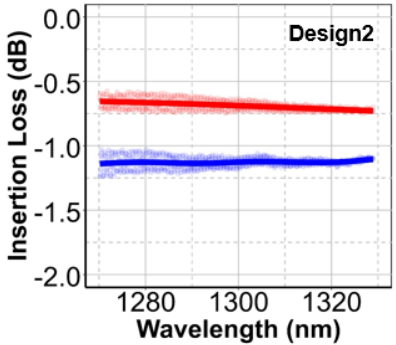
- ❑ **SiN edge coupler module (127-um pitch) passed full reliability assessments**
  - Chip-fiber-package (CFP) qualification leveraging 36 modules
  - Extensive reliability tests exceeding Telcordia specification GR-468 requirements
  - IL delta **< 0.5 dB** for both polarizations before and after reliability test – indicating no obvious systematic degradation mechanism.

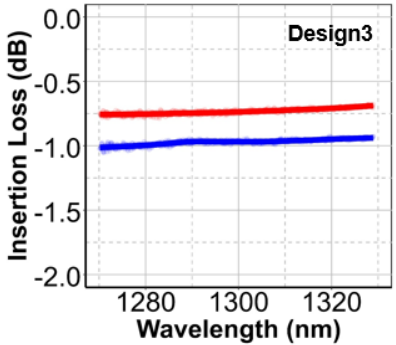
LTS: Low Temperature Storage
HTS: High Temperature Storage
TC: Temperature Cycling
DH: Damp Heat

Multi-tip SiN edge coupler for further IL reduction



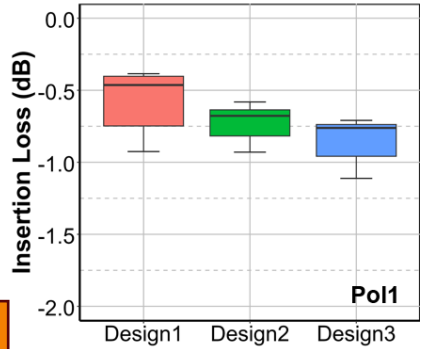


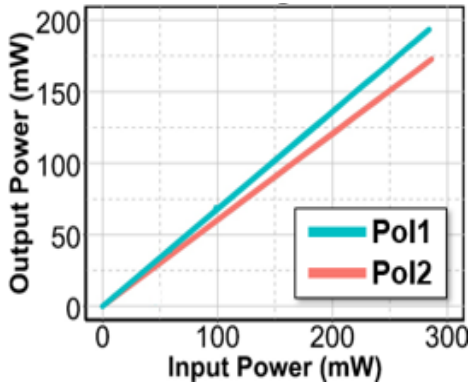




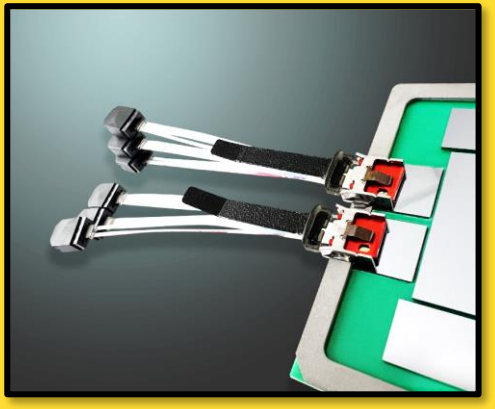
- Broadband high-power V-groove based multi-tip SiN edge coupler
  - **Lowest insertion loss reported**: **~0.4 dB**
  - Low polarization dependent loss: **< 0.25 dB**
  - Low wavelength dependence: **< 0.2 dB**
  - Low optical return loss: **< -40 dB**
  - Good high-power handling: **expect > 520 mW**

IL as low as 0.4 dB @ O-band – lowest reported on 300-mm monolithic SiPh platform





Source: *Y. Bian, et al., OFC, M4J.6 (2025).*



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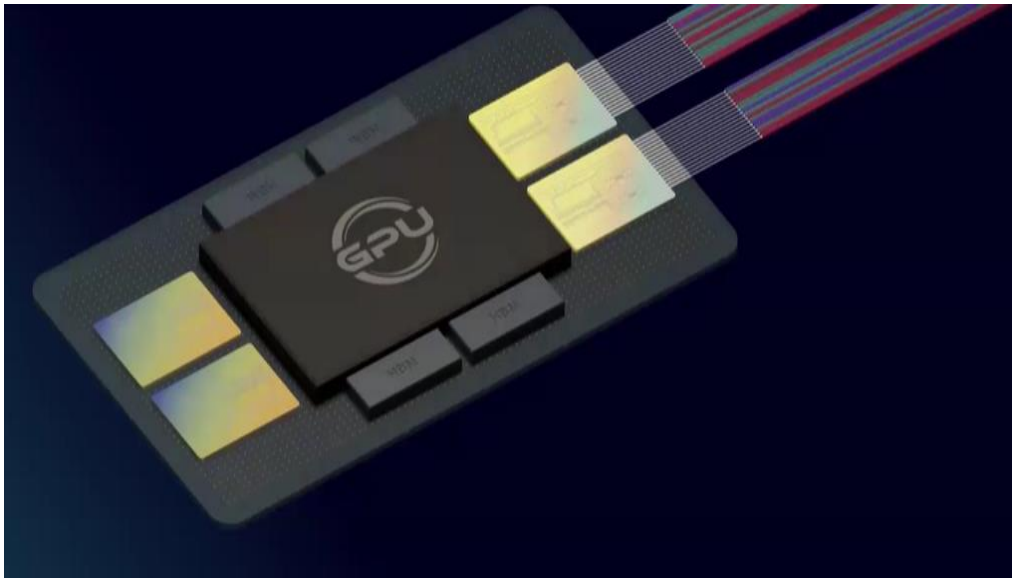
Fiber attach challenge for CPO & 2.5D integration



Challenges	Details
2.5D fiber integration	Photonics+Logic+HBM, Thinned PIC with TSV, reflow compatibility
Bandwidth scalability	Fiber counts, shoreline high density
Mechanics reliability	Form factor, mechanical stresses, warpage, fiber handling and routing
Thermal reliability	High temp, colling
Manufacturability	Reworkability, cleanness, testability
Ecosystem combability	Supply chain flow, foundry, cost

- Source: https://teramount.com/
- H. Taha, Scalable Detachable Fiber Connectivity for Seamless Integration With Advanced Semiconductor Packaging, OFC, W4A.3 (2025).

Teramount Detachable Fiber Connectivity Solution

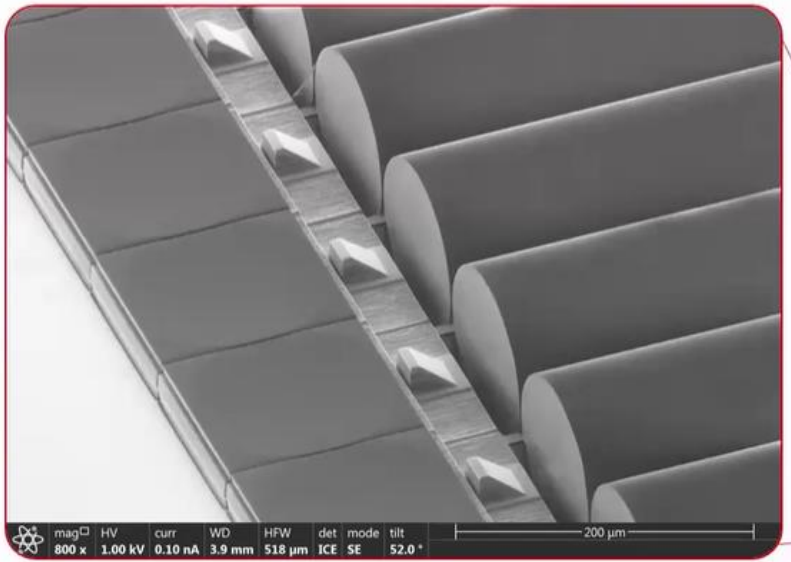
2.5D Packaging Architectures

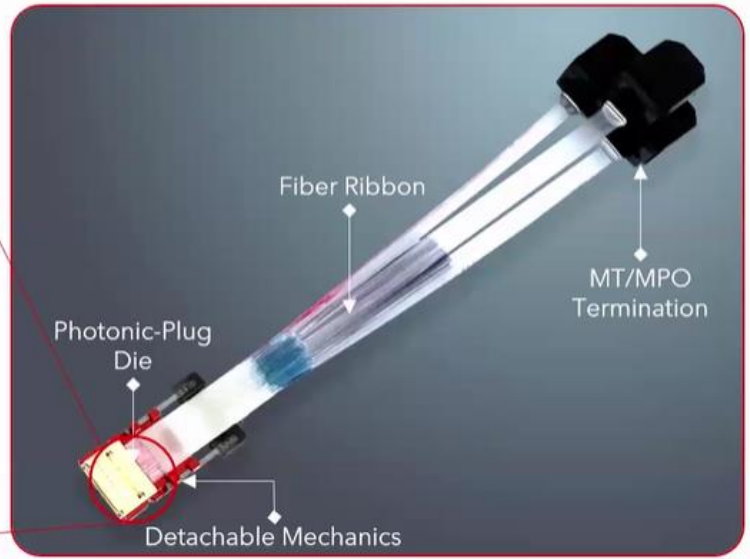
Detachable Fiber Connector, 10's Fibers, 127um pitch

Large Fiber Count for Highest Bandwidth Density

- Source: https://teramount.com/
- H. Taha, Scalable Detachable Fiber Connectivity for Seamless Integration With Advanced Semiconductor Packaging, OFC, W4A.3 (2025)

Photonic-Plug fiber connector

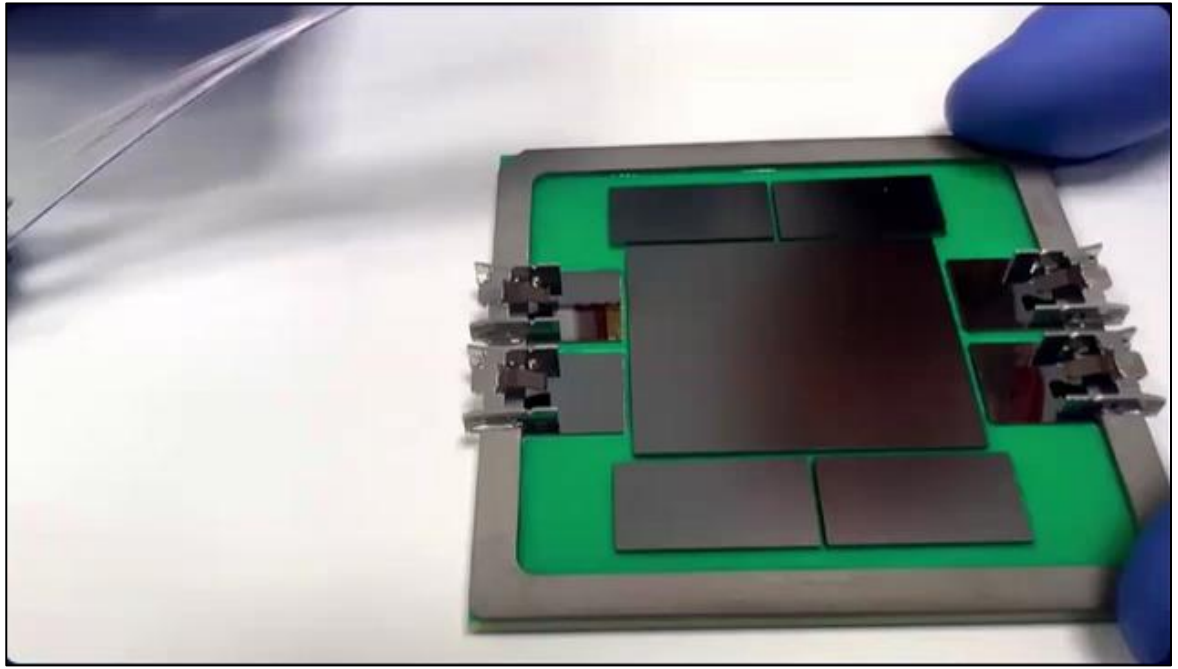




- Wafer level fabrication process enabling high accuracy photonic-plug interfacing with SMF/PMF
  - Large fiber account: 10's SMF/PMF

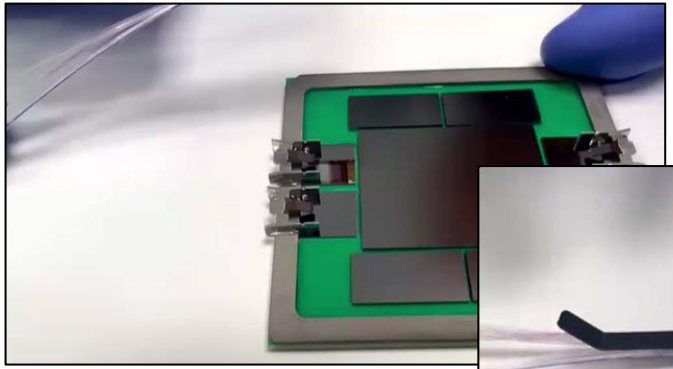
- Source: https://teramount.com/
- H. Taha, Scalable Detachable Fiber Connectivity for Seamless Integration With Advanced Semiconductor Packaging, OFC, W4A.3 (2025).

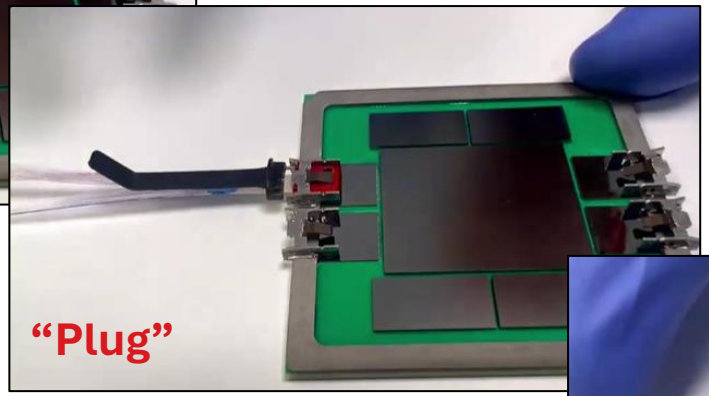
Photonic-Plug fiber connector

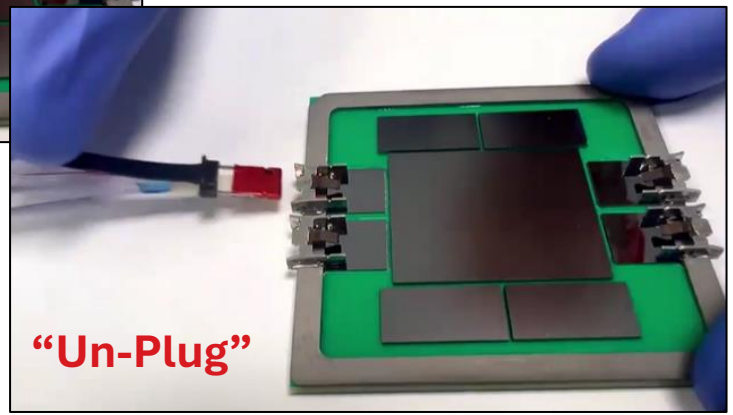


- Demo showing how the photonic plug fiber connector can be plugged and unplugged into a SiPh die which includes photonic circuits and mechanical elements

Photonic-Plug fiber connector

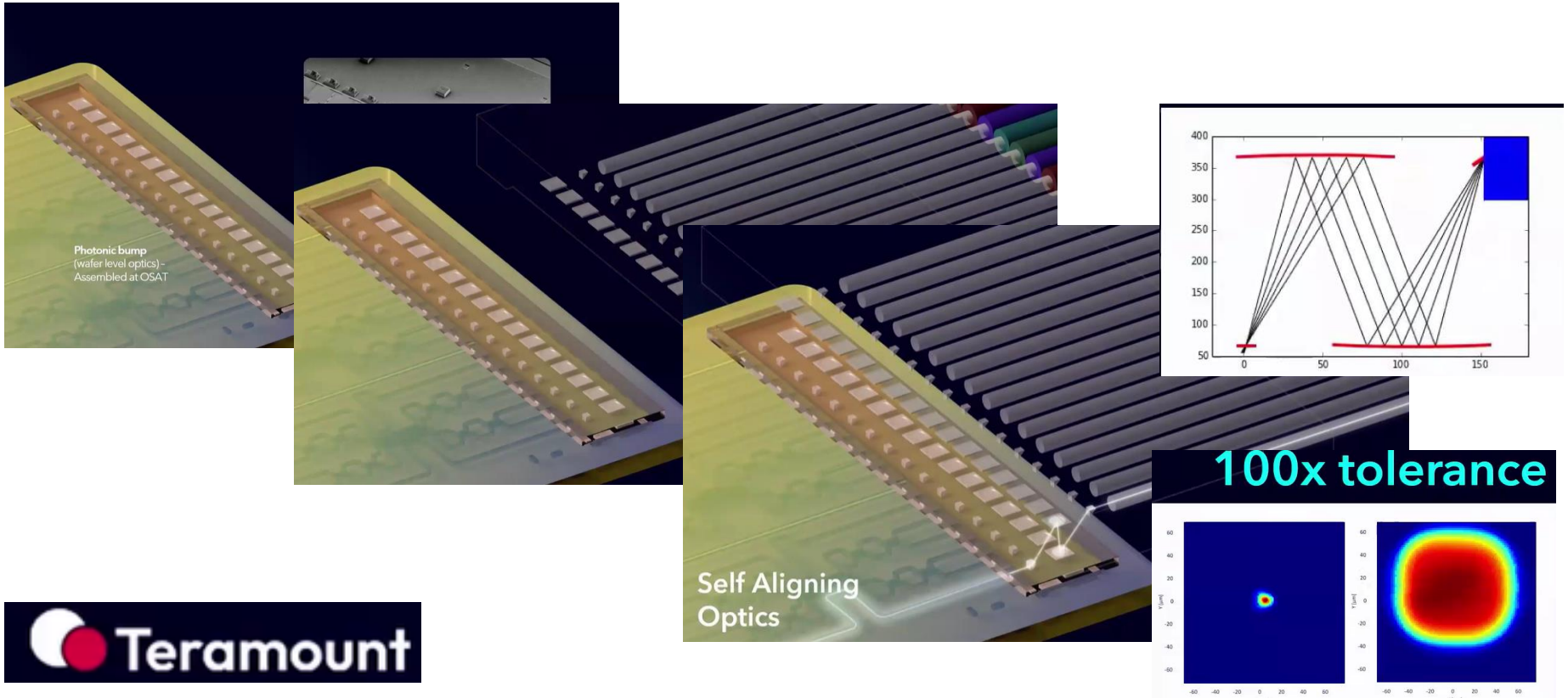






- Demo showing how the photonic plug fiber connector can be plugged and unplugged into a SiPh die which includes photonic circuits and mechanical elements

Detachable I/O coupler with Photonic-Plug & Photonic-Bump



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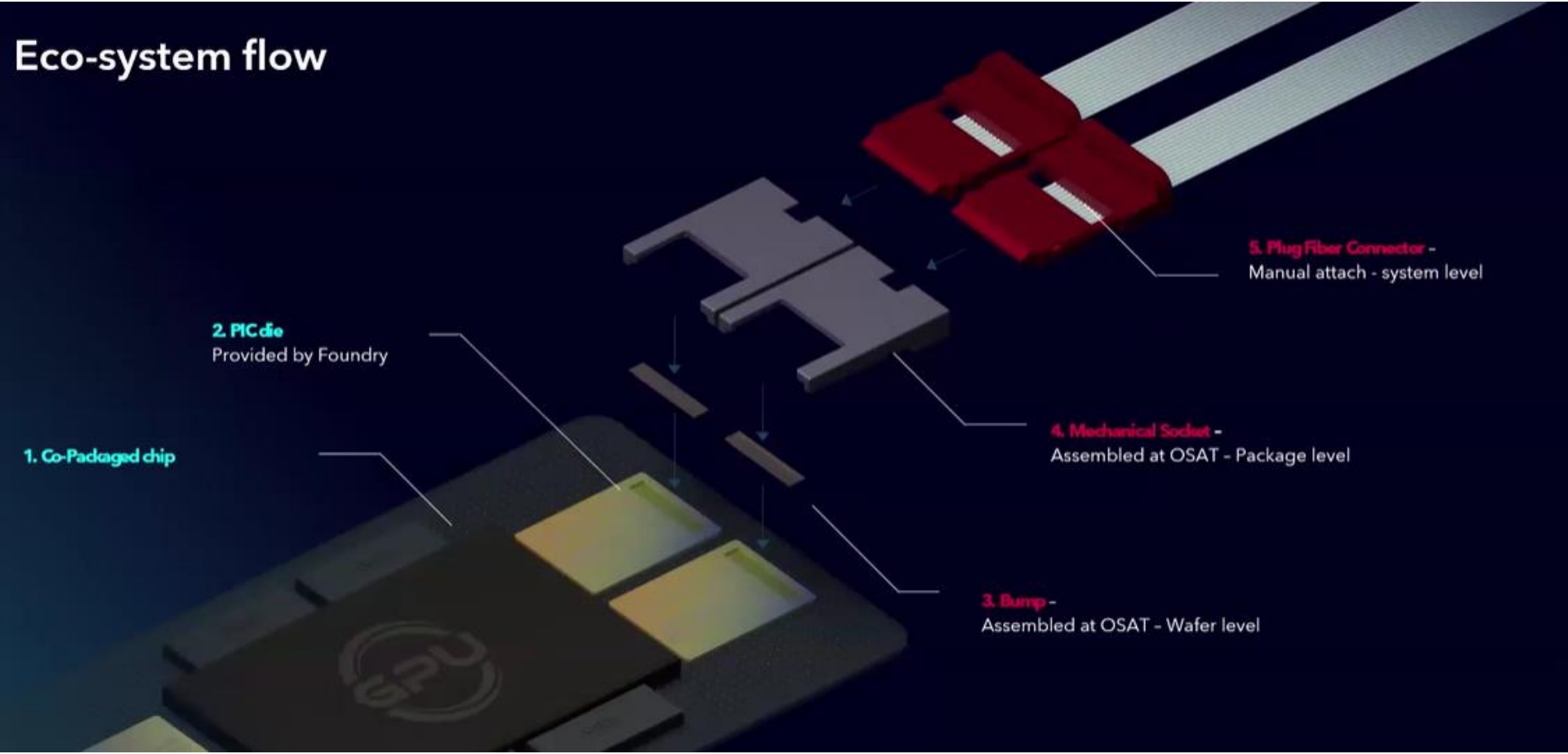
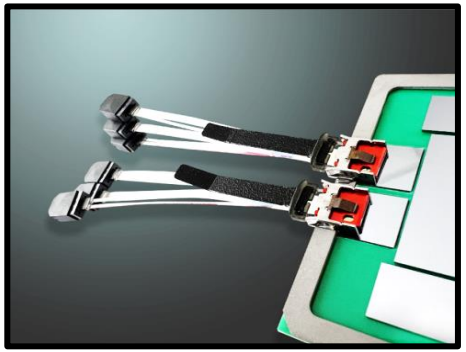
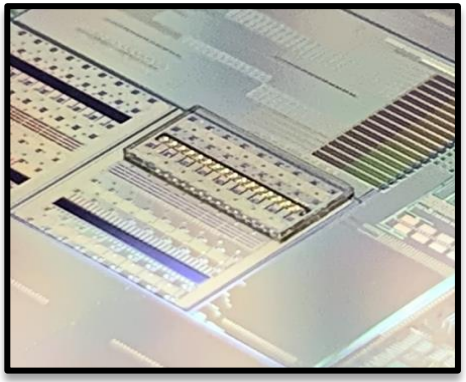
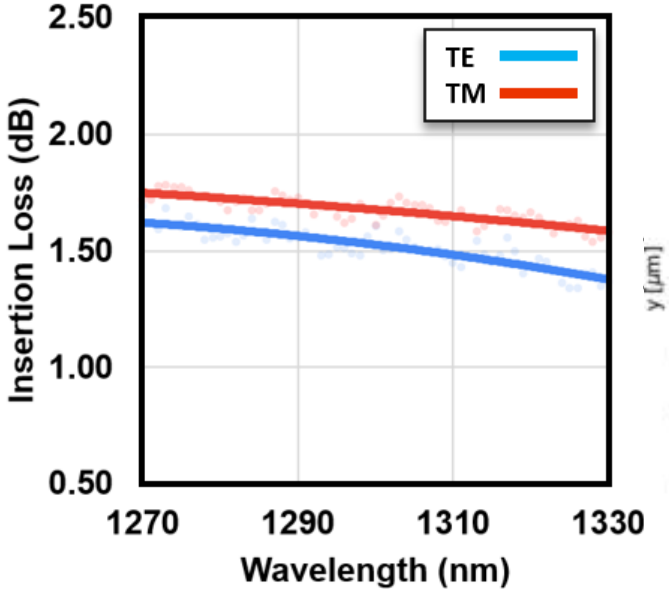
Eco-system flow

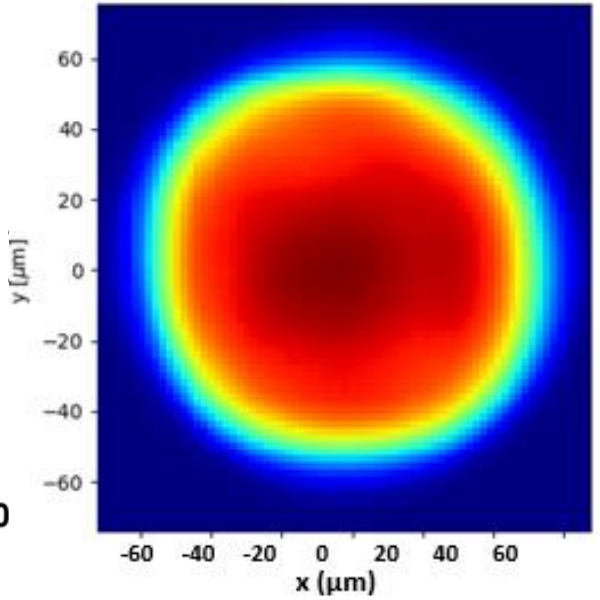


Detachable I/O coupler performance on GF platform









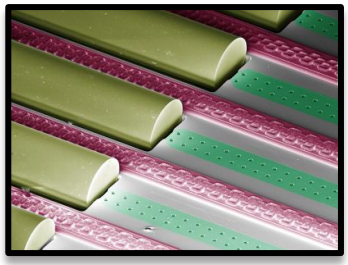
- Wafer-level detachable I/O solution (“reworkable”)
  - **Sub 1.8 dB IL** and broadband performance (flat through-band)
  - **+/- 30 um 0.5 dB** misalignment tolerance
  - **+/- 45 um 1 dB** misalignment tolerance

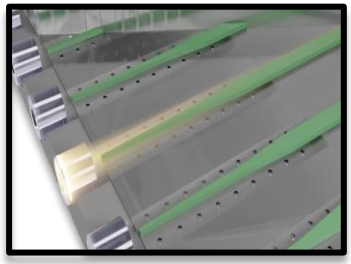
Source: *Y. Bian, et al., CLEO AA129.1 Invited talk (2025)*

1	GF monolithic SiPh platform
2	V-groove-based fiber attach
3	Detachable I/O coupler
4	Summary and outlook

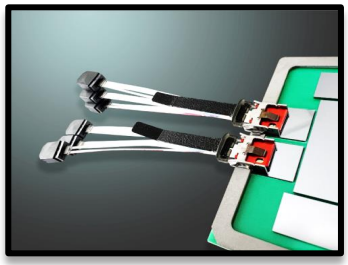
Summary and outlook

V-groove fiber attach





Detachable I/O coupler



- Mass-manufacturable high-performance and diverse optical I/O solutions on 300-mm monolithic CMOS-SiPh platform for CPO and AI data center applications
- V-groove fiber attach
  - **250 um** and **127 um** pitch V-groove options
  - Single and multi-tip SiN edge couplers
  - IL as low as **0.4 dB**, PDL as low as **0.1 dB**
  - **ORL < -40 dB**
  - Power handling **> 520 mW**
- Detachable I/O coupler
  - Wafer-level detachable solution
  - **Sub 1.8 dB IL** and broadband performance
  - **+/- 30 um 0.5 dB** misalignment tolerance
  - **+/- 45 um 1 dB** misalignment tolerance
- Outlook
  - Continue to push beach front density
  - Continue to reduce IL for all solutions
  - Continue to drive performance improvement

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